CLAIMS

What is claimed is:

1. An integrated circuit chip package comprising:

a metal substrate core including,

a first region, and

a second region electrically isolated from the first region.

2. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with an operating voltage rail of an integrated circuit chip.

3. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with a digital ground of an integrated circuit chip.

4. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with an analog ground of an integrated circuit chip.

5. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with an operating voltage rail of an integrated circuit chip, and at least one other of the regions of the substrate core is coupled with a digital ground of the integrated circuit chip.

6. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with an operating voltage rail of an integrated circuit chip, and at least one other of the regions of the substrate core is coupled with an analog ground of the integrated circuit chip.

7. The integrated circuit chip package of claim 1, wherein at least one of the regions of the substrate core is coupled with a digital ground of an integrated circuit chip, and at least one other of the regions of the substrate core is coupled with an analog ground of the integrated circuit chip.

8. An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least two electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip.

9. The integrated circuit chip package of claim 8, further comprising:

input and output signals of the integrated circuit chip routed through the electrically isolated region of the metal substrate core that is coupled with the digital ground of the integrated circuit chip.

10. The integrated circuit chip package of claim 9, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

11. The integrated circuit chip package of claim 9, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

12. An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least three electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip and has input and output signals routed through it.

13. The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

14. The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

15. The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip, and at least one other of the electrically isolated region of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

16. A method comprising:

creating initial clearances on a metal substrate core that do not fully electrically separate the core into two ore more regions;

filling the initial clearances with dielectric material; and

creating final clearances that fully electrically separate the two or more regions of the metal substrate core.

17. The method of claim 16, further comprising filling the final clearances with dielectric material.

18. The method of claim 16, wherein creating the initial or final clearances comprises chemical etching.

19. The method of claim 16, wherein creating the initial or final clearances comprises laser etching.

20. The method of claim 16, wherein creating the initial or final clearances comprises mechanical methods including at least one of drilling, routing, and punching.